FIG.1 THE PRESENT INVENTION

SIGNAL NAME	LOGICAL EXPRESSION /FETCHING EDGE	SIGNAL SPEED (IN TERMS OF FREQUENCY)
Din		f/2
CK1	CK	f/2
CK2	CKN	f/2
q1	↑ CK1	f/3
q2	↑ CK2	f/3
q3	↑ CK2	f/4
q4	↑ CK1	f/4
Error1	q2 xor q3	<f/2
Error2	q1 xor q4	<f/2
Ref1	(q3 xor q4)*CK2	<f/2
Ref2	(q3 xor q4)*CK1	<f/2

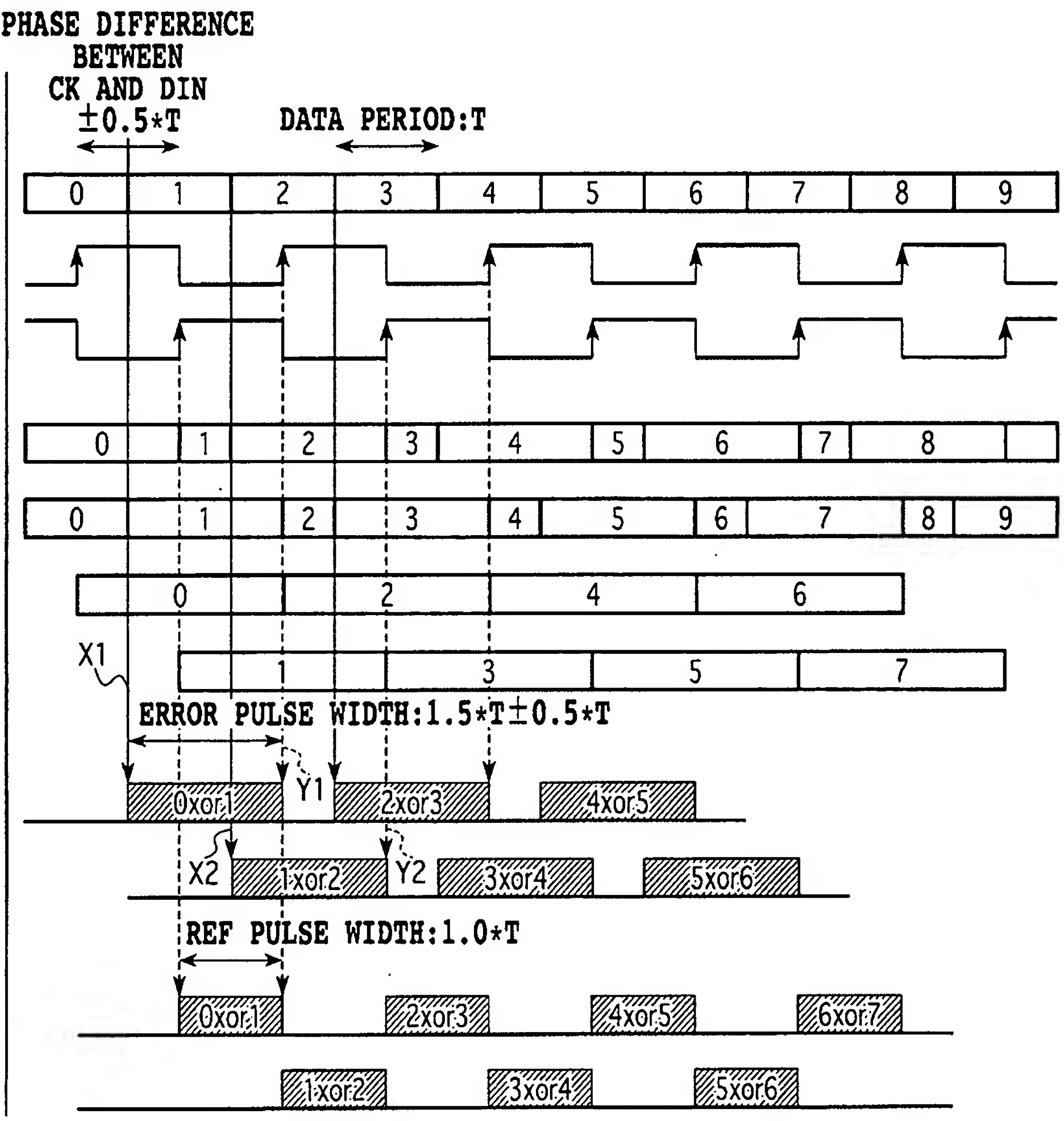


FIG.2

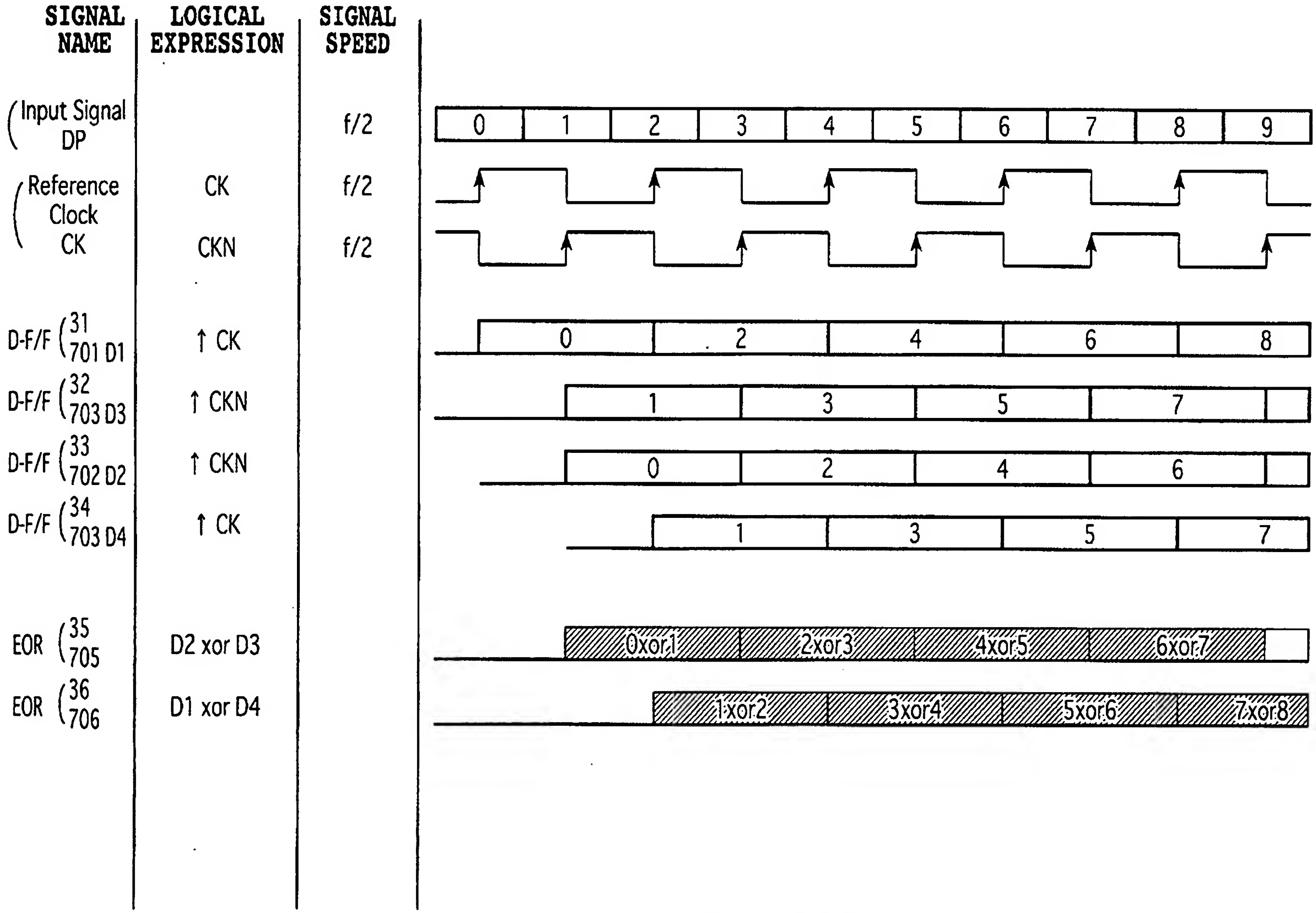

SIGNAL NAME
LOGICAL EXPRESSION
SIGNAL SPEED
Input Signal DP
f/2
0
1
2
3
4
5
6
7
8
9
Reference Clock CK
CK
f/2
CKN
f/2
D-F/F 31 701 D1
↑ CK
0
2
4
6
8
D-F/F 32 703 D3
↑ CKN
1
3
5
7
D-F/F 33 702 D2
↑ CKN
0
2
4
6
D-F/F 34 703 D4
↑ CK
1
3
5
7
EOR 35 705
D2 xor D3
0xor1
2xor3
4xor5
6xor7
EOR 36 706
D1 xor D4
1xor2
3xor4
5xor6
7xor8

FIG.3 THE PRESENT INVENTION

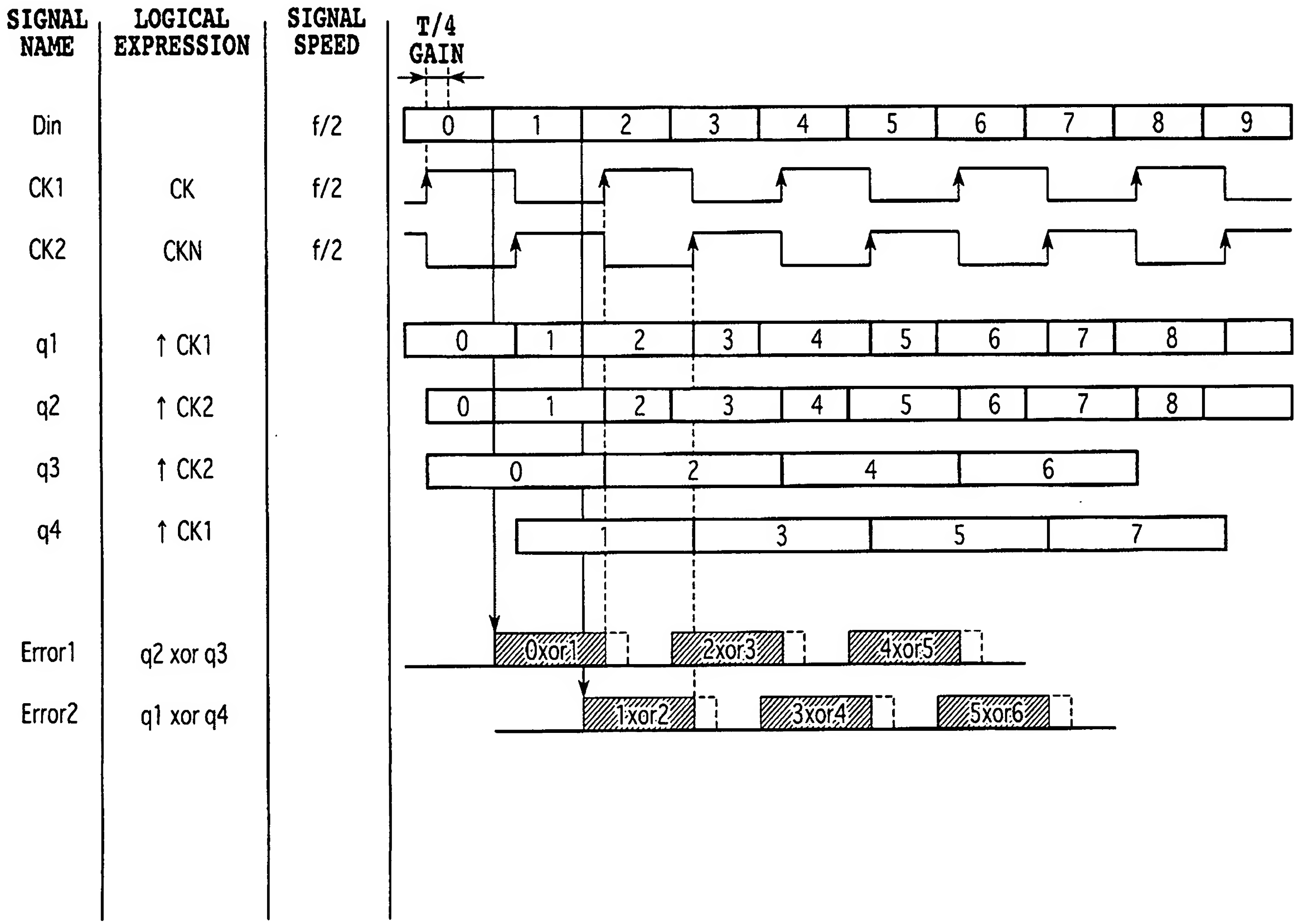


FIG.4 HOLMQVIST AND SUMMERS

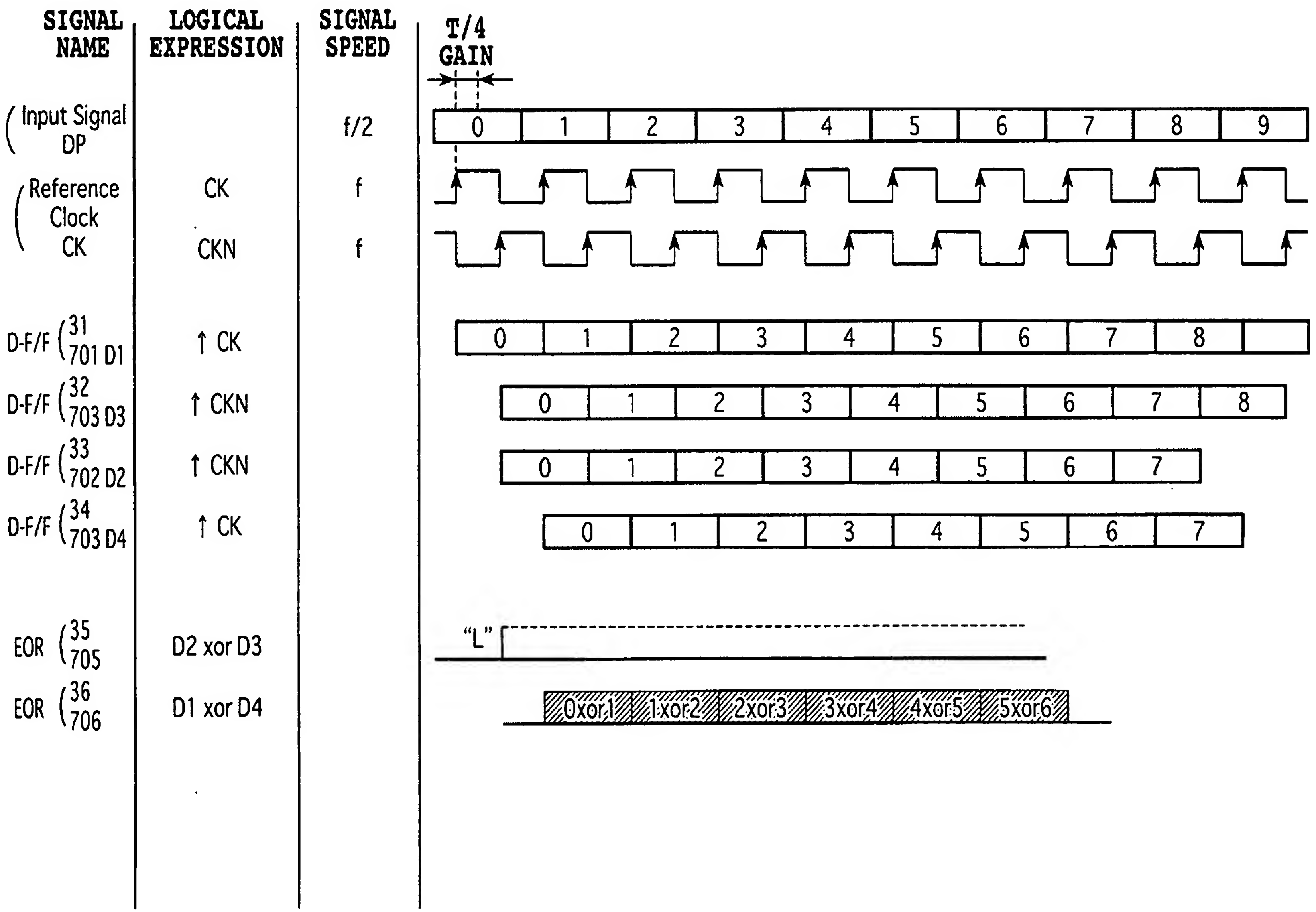


FIG.5 THE PRESENT INVENTION

SIGNAL NAME	LOGICAL EXPRESSION	SIGNAL SPEED
Din		f/2
CK1	CK	f/2
CK2	CKN	f/2
q1	↑ CK1	
q2	↑ CK2	
q3	↑ CK2	
q4	↑ CK1	
Error1	q2 xor q3	
Error2	q1 xor q4	

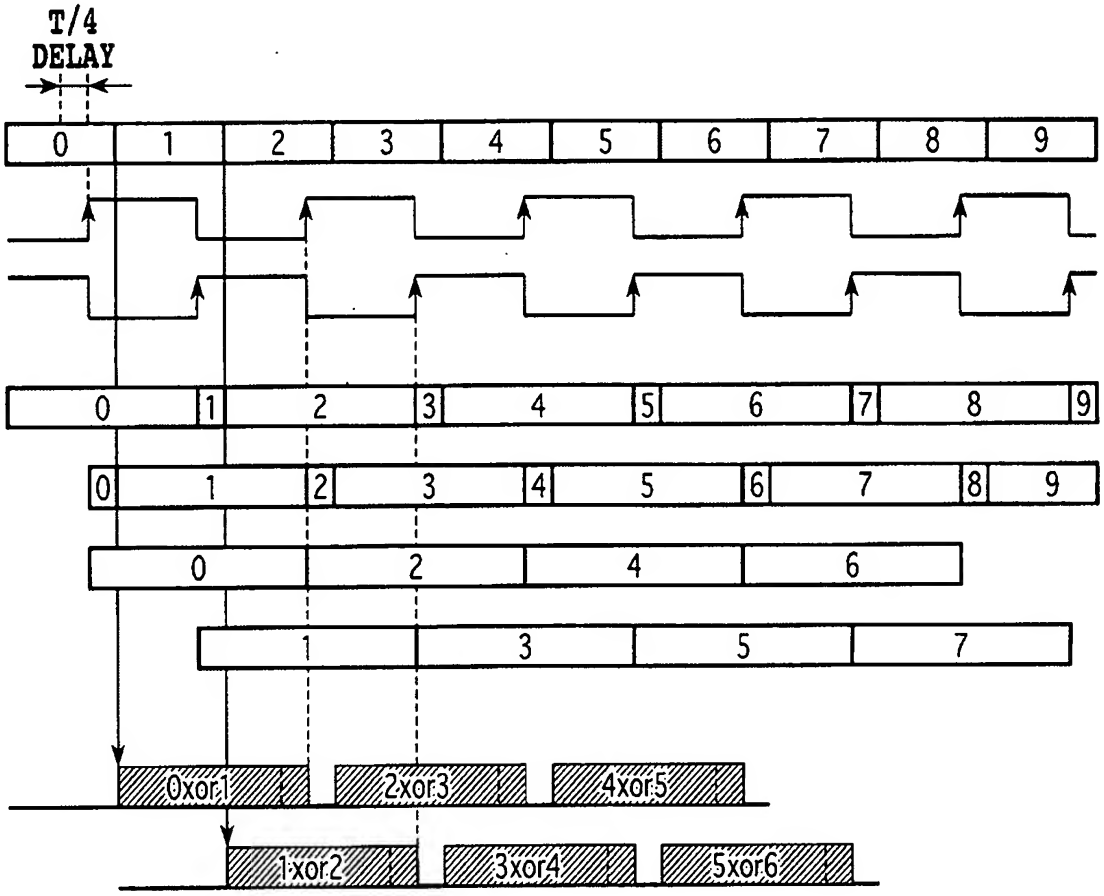
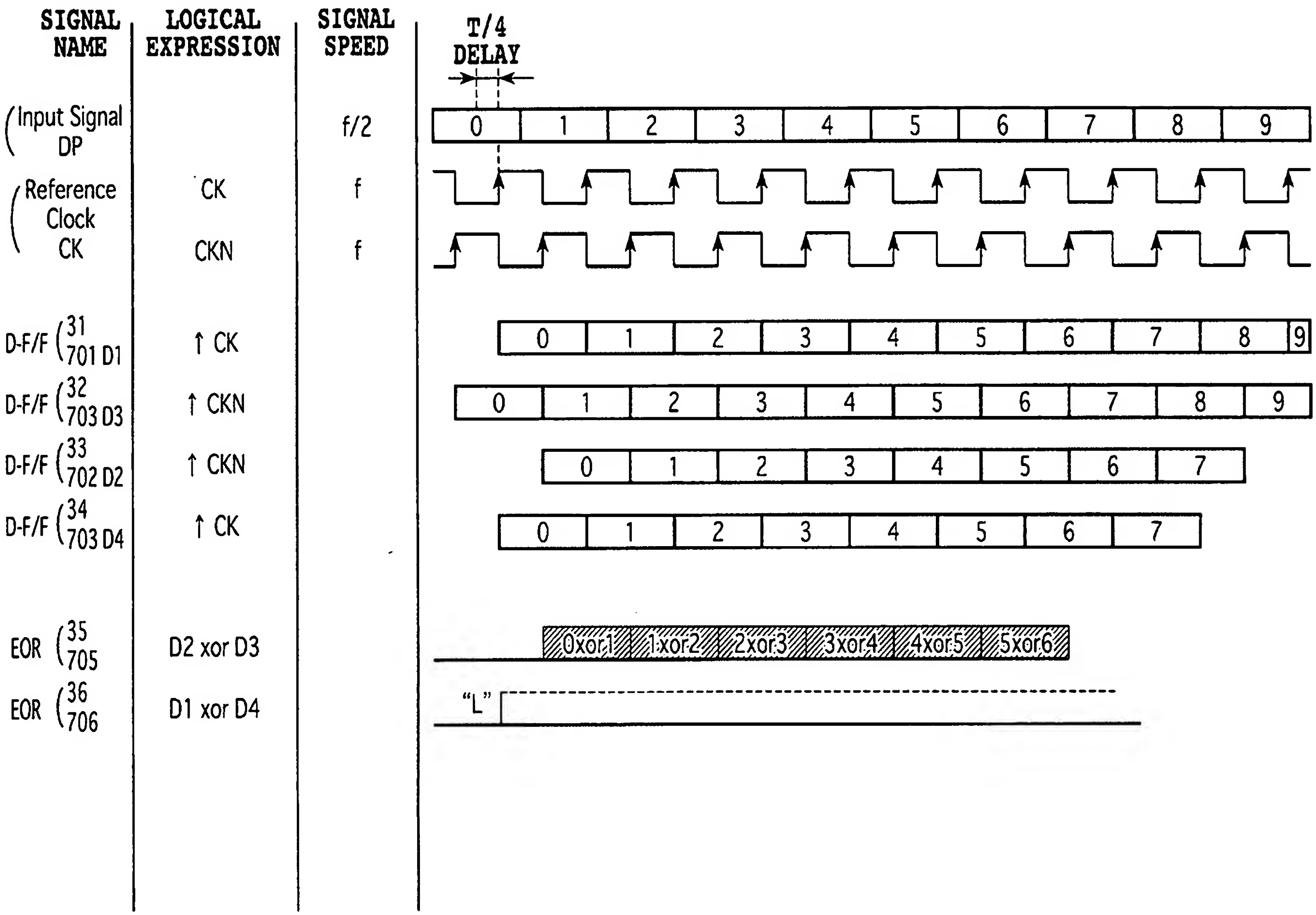


FIG.6


SIGNAL NAME
LOGICAL EXPRESSION
SIGNAL SPEED
T/4 DELAY
Input Signal DP
f/2
0
1
2
3
4
5
6
7
8
9
Reference Clock CK
CK
f
CKN
f
D-F/F 31 701 D1
↑ CK
D-F/F 32 703 D3
↑ CKN
D-F/F 33 702 D2
↑ CKN
D-F/F 34 703 D4
↑ CK
EOR 35 705
D2 xor D3
0xor1
1xor2
2xor3
3xor4
4xor5
5xor6
EOR 36 706
D1 xor D4
"L"